CLAIMS

We Claim:

1. An apparatus comprising:

a controller to couple to a data bus and to a plurality of devices to transfer data between the devices and the data bus in response to a command signal, said controller to generate a chip select signal to select a particular device from the plurality of devices to respond to the command signal; and

a logic unit coupled to generate a command occurrence signal based on timing of chip select signals to identify when command signals occur, the command occurrence signal to be asserted prior to the chip select signals to allow a flag signal to complete a data transfer.

2. The apparatus of claim 1 wherein the command occurrence signal, chip select signal and the flag signal are coupled to a table entry in the particular device, so that an indication of a presence of all three signals causes a trigger signal to be generated in the particular device to execute the data transfer.

3. The apparatus of claim 2 wherein the table entry is to be cleared after receiving the flag signal to allow said table entry to receive next set of command occurrence, chip select and flag signals to determine if the trigger signal is to be generated for the particular device with the next set of command occurrence, chip select and flag signals.

4. The apparatus of claim 3 wherein the flag signal to indicate timing of the data transfer occurs with positive and negative transitions of the flag signal.

5. The apparatus of claim 3 wherein said memory is a dynamic-random-access-memory, DRAM.

6. The apparatus of claim 1 wherein the command signal is a read or write command signal for a memory device.

7. An apparatus comprising:

a memory to couple to a data bus to transfer data between said memory and bus in response to a command signal received to initiate data transfer and a flag signal received to complete the data transfer, said memory to operate as one of a plurality of memories in which a chip select signal selects said memory from the plurality of memories and wherein a flag signal operating in timing order with a command occurrence signal, which is based on timing of chip select signals to the plurality of memories, indicates timing when the data transfer is to occur following the command occurrence signal, the command occurrence signal to be asserted prior to the chip select signals to allow the flag signal to complete the data transfer; and

a timing unit coupled to receive the command occurrence signal, flag signal and the chip select signal, said timing unit to generate a trigger signal in response to the flag signal to execute the data transfer, if the command occurrence signal and the chip select signal indicate that said memory is selected for the data transfer.

8. The apparatus of claim 7 wherein the command signal is a read command or write command.

9. The apparatus of claim 8 wherein the command occurrence signal is a rank select signal to select a rank of memory containing the memory to be selected by the chip select signal.

10. The apparatus of claim 9 wherein said timing unit includes table entries to maintain record of the rank select signal, chip select signal and the flag signal, so that a rank entry is to be set when the rank select command is present, a chip select entry is to be set when the chip select signal is present and the flag entry is to be set when the flag signal is present, the trigger signal to be generated to execute the data transfer when all three respective entries are set.

11. The apparatus of claim 10 wherein the respective table entries are to be cleared after receiving the flag signal to allow the entries to receive a next set of rank select, chip select and flag signals.

12. The apparatus of claim 11 wherein the flag signal to indicate timing of the data transfer occurs with positive and negative transitions of the flag signal.

13. The apparatus of claim 12 wherein said memory is a dynamic-random-access-memory, DRAM.

14. The apparatus of claim 9 wherein said timing unit includes table entries arranged in a queue to maintain record of occurrences of the rank select, chip select and the flag signals, so that subsequent occurrences of all three signals is to be recorded.

15. The apparatus of claim 14 further includes a first pointer to point to a next set of entries after recording the occurrence of the rank select and chip select signals; and a second pointer to point to the next set of entries after recording the occurrence of the flag signal.

16. The apparatus of claim 14 wherein said memory is a dynamic-random-access-memory, DRAM.

17. A system comprising:

a controller to generate a command signal to initiate a data transfer in response to the command signal, said controller to generate a chip select signal, a rank select signal and a flag signal associated with the command signal;

a bus coupled to said controller; and

a plurality of memories coupled to said bus to transfer data between said memories and bus in response to the command signal generated by said controller, one of said plurality of memories being selected by the chip select signal for the data transfer in which the flag signal times the execution of the data transfer and the rank select signal times the occurrence of the command signal, the rank select signal to be asserted prior to the chip select signal to allow the flag signal to complete the data transfer.

18. The system of claim 17 wherein one of said memories includes a timing unit, in which table entries in the timing unit maintains record of the rank select signal, chip select signal and the flag signal, so that a rank select entry is to be set when the command signal is a read or write command, a chip select entry is to be set when the chip select signal is

present and the flag entry is to be set when the flag signal is present, and a trigger signal to be generated to execute the data transfer when all three respective entries are set.

19. The system of claim 18 wherein the respective table entries are to be cleared after receiving the flag signal to allow the entries to receive a next set of rank select, chip select and flag signals.

20. The system of claim 19 wherein the flag signal to indicate timing of the data transfer occurs with positive and negative transitions of the flag signal.

21. The system of claim 19 wherein said memory is a dynamic-random-access-memory, DRAM.

22. A method comprising:

issuing a command signal to perform a read or write operation;

issuing a chip select signal to select a particular memory device from a plurality of devices to perform a data transfer for the read or write operation;

issuing a command occurrence signal to identify when the command signal is generated, the command occurrence signal being generated prior to the chip select signal;

generating a flag signal subsequently in response to the issuing of the command signal to complete the data transfer; and

capturing occurrences of the command occurrence signal, chip select signal and the flag signal in a memory device and generating a trigger signal when command occurrence, chip select and flag signals present are captured for the memory device, the trigger signal to execute the data transfer to complete the read or write operation in the memory device.

23. The method of claim 22 wherein the command occurrence signal is asserted one clock period prior to the chip select signal being asserted.

24. The method of claim 23 wherein said capturing the signals are achieved by setting entries on occurrence of the signals.

25. The method of claim 24 further including the clearing of the entries after occurrence of the flag signal.

26. The method of claim 23 wherein said capturing of the signals is performed in a dynamic-random-access-memory, DRAM.